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Amendments to the Claims

- 1. (Previously presented) A process for forming a copper interconnect in a substrate including a connect hole vertically extending through an inter-level dielectric layer, comprising the steps of:
- a first step, performed at least partially by atomic layer deposition, of depositing a barrier layer comprising tantalum on sides of said hole;
- a second step of etching said barrier layer at a bottom of said hole selectively to said barrier layer on said sides of said hole;
- a subsequent third step, performed by physical vapor deposition, of depositing a copper seed layer over said barrier layer; and

filling by electrochemical plating copper into said hole over said copper seed layer.

- 2. (Original) The process of Claim 1, wherein said barrier layer comprises tantalum nitride.
 - 3. (Cancelled)

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- 4. (Previously presented) A process for forming a copper interconnect in a substrate including a connect hole vertically extending through an inter-level dielectric layer, comprising the steps of:
- a first step, performed at least partially by atomic layer deposition, of depositing a barrier layer comprising tautalum on sides of said hole;
- a subsequent second step of etching said barrier layer at the bottom of the hole, wherein second step includes generating an argon plasma and biasing a pedestal electrode supporting said substrate to attract argon ions to said substrate, thereby etching said barrier layer;
 - a subsequent third step, performed by physical vapor deposition, of depositing a copper

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seed layer over said barrier layer; and

filling by electrochemical plating copper into said hole over said copper seed layer.

- 5. (Original) The process of Claim 4, wherein said generating step includes inductively coupling RF power into a plasma reactor containing said pedestal electrode.
- 6. (Previously presented) A process for forming a copper interconnect in a substrate including a connect hole vertically extending through an inter-level dielectric layer, comprising the steps of:
- a first step, performed at least partially by atomic layer deposition, of depositing a barrier layer comprising tantalum on sides of said hole, wherein said first step includes an initial CVD step for depositing a first part of said barrier layer and a subsequent sputtering step for depositing a second part of said barrier layer;
- a second step, performed by physical vapor deposition, of depositing a copper seed layer over said barrier layer; and

filling by electrochemical plating copper into said hole over said copper seed layer.

- 7. (Original) A process for forming a copper interconnect in a substrate including a connect hole vertically extending through an inter-level dielectric layer, comprising the sequentially performed steps of:
- a first step, performed by chemical vapor deposition, of depositing a first barrier layer comprising tantalum on sides of said hole:
- a second step, performed by sputtering, of depositing a second barrier layer comprising tantalum on said sides of said hole;
- a third step, performed by physical vapor deposition, of depositing a copper seed layer over said first and second barrier layers; and
- a fourth step, performed by electrochemical plating, of filling copper into said hole over said copper seed layer.

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- 8. (Previously presented) The process of Claim 7, wherein said chemical vapor deposition comprises atomic layer deposition.
- 9. (Original) The process of Claim 7, further comprising a fifth step performed after said first step performed in a sputter reactor of etching said first barrier layer at the bottom of said hole.
- 10. (Original) The process of Claim 9, wherein fifth step includes generating an argon plasma and biasing a pedestal electrode supporting said substrate to attract argon ions to said substrate, thereby etching said barrier layer.
- 11. (Original) The process of Claim 10, wherein said generating step includes inductively coupling RF power into a plasma reactor containing said pedestal electrode.
 - 12. (Canceled)
- 13. (Original) A process for forming a copper interconnect in a substrate including a connect hole vertically extending through an inter-level dielectric layer, comprising the steps of:

depositing by a deposition process comprising chemical vapor deposition a nitrided barrier layer on sides of said hole;

in a sputter reactor including a tantalum target, etching said nitrided barrier layer on a bottom of said hole;

in said sputter reactor, depositing a material comprising tantalum on sidewalls of said hole to form a second barrier layer;

depositing by physical vapor deposition a copper seed layer over said second barrier layer; and

filling by electrochemical plating copper into said hole over said copper seed layer.

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- 14. (Original) The process of Claim 13, wherein said deposition process comprises atomic layer deposition.
- 15. (Original) The process of Claim 13, wherein said nitrided barrier layer comprises TiSiN.
- 16. (Original) The process of Claim 13, wherein said second barrier layer comprises TaN.

17-41. (Canceled)

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- 42. (Previously presented) A method of filling one or more of a via and a trench in a patterned substrate, comprising:
- a) depositing a generally conformal first barrier layer in one or more of the via and the trench on the patterned substrate by chemical vapor deposition, wherein the first barrier layer comprises a silicided nitride of a refractory metal selected from the group consisting of Ti, Ta, and W;
 - b) removing the first barrier layer from horizontal surfaces of the patterned substrate;
 - c) depositing a second barrier layer by physical vapor deposition; and
 - d) then depositing one or more conductive materials.
- 43. (Previously presented) The method of Claim 42, wherein depositing the conductive material comprises depositing a seed layer and a metal layer in the via and/or the trench after the second barrier layer is deposited.
- 44. (Previously presented) The method of Claim 43, wherein the first barrier layer comprises a material is selected from the group consisting of Ti, Ta, W, and nitrides thereof.

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- 45. (Previously presented) The method of Claim 42, wherein the second barrier layer comprises at least one refractory metal selected from the group consisting of Ta and W.
- 46. (Previously presented) The method of Claim 43, wherein the seed layer comprises copper.
- 47. (Previously presented) The method of Claim 46, wherein the metal layer comprises is copper.

48-49. (Canceled)

- 50. (Previously presented) The method of Claim 43, wherein the seed layer is deposited by physical vapor deposition.
- 51. (Canceled) The method of Claim 43, wherein the metal layer is deposited by chemical vapor deposition.
- 52. (Previously presented) The method of Claim 43, wherein the metal layer is deposited by electroplating.
- 53. (Previously presented) The method of Claim 42, wherein the second barrier layer comprises a material selected from the group consisting of Ta, TaN, W, WN, Ti, and TiN, and wherein the second barrier layer has a thickness of from about 2nm to about 5nm at the bottom of the via.
- 54. (Previously presented) A method of filling one or more holes in a patterned substrate, comprising:
 - a) depositing a generally conformal first barrier layer on the patterned substrate by atomic

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layer deposition;

- b) removing the first barrier layer from horizontal surfaces of the patterned substrate;
- c) depositing a second barrier layer by physical vapor deposition; and
- d) then depositing one or more conductive materials to fill the holes.
- 55. (Previously presented) The method of Claim 54, wherein depositing the conductive material comprises depositing a seed layer and a metal layer in the holes after the second barrier layer is deposited.
- 56. (Previously presented) The method of Claim 55, wherein the first barrier layer comprises a material selected from the group consisting of Ta, TaN, W, and WN.
- 57. (Previously presented) The method of Claim 56, wherein the second barrier layer comprises a material selected from the group consisting of Ta, TaN, T, TiN, W, and WN.
- 58. (Previously presented) The method of Claim 57, wherein the seed layer comprises copper.
- 59. (Previously presented) The method of Claim 58, wherein the metal layer comprises copper.
- 60. (Previously presented) The method of Claim 55, wherein the seed layer is deposited by physical vapor deposition.
- 61. (Previously presented) The method of Claim 55, wherein the metal layer is deposited by electroplating.
 - 62. (Previously presented) The method of Claim 54, wherein the second barrier layer

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comprises a material selected from the group consisting of Ta, TaN, W, WN, Ti, and TiN.

63. (Canceled)

- 64. (Currently amended) The method of Claim 63 A method of filling one or more of a via and a trench in a patterned substrate, comprising:
- a) depositing a generally conformal first barrier layer on the patterned substrate by chemical vapor deposition:
 - b) removing the first barrier layer from the horizontal surfaces of the patterned substrate;
 - c) depositing a second barrier layer by physical vapor deposition; and
- d) then depositing one or more conductive materials, wherein depositing the conductive material comprises depositing a seed layer and a metal layer in the via and/or the trench after the second barrier layer is deposited.
- 65. (Previously presented) A method of filling one or more of a via and a trench in a patterned substrate having a metal layer underlying the via, comprising:
- a) depositing a generally conformal first barrier layer on the patterned substrate by chemical vapor deposition, wherein the first barrier layer comprises a silicided nitride of a refractory metal selected from the group consisting of Ti, Ta, and W;
 - b) removing the first barrier layer from horizontal surfaces of the patterned substrate;
- c) depositing by physical vapor deposition a second barrier layer sufficient to provide a barrier on the bottom of the trench; and
 - d) then depositing one or more conductive materials.
- 66. (Previously presented) A method of filling one or more of a via and a trench in a patterned substrate having a metal layer underlying the via, comprising:
- a) depositing a generally conformal first barrier layer on the patterned substrate by atomic layer deposition;

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 b) removing the first barrier layer from horizontal surfaces of the patterned substrate;
 c) depositing by physical vapor deposition a second barrier layer sufficient to provide a

 barrier on a bottom of the trench; and
 d) then depositing one or more conductive materials.

 67. (Currently amended) The process of claim [[3]] L, wherein said etching is perform with energetic ions.

 PAGE 13/15* RCVD AT 5/12/845 1:31:20 PM [Eastern Dayloght Time]* SYR-USPTO-EFARF-1/25* DNR-2731694* CSID-690 588 8042* DURATION (numes):04-28 c) depositing by physical vapor deposition a second barrier layer sufficient to provide a

 - 67. (Currently amended) The process of claim [[3]] 1, wherein said etching is performed